

MAT-6660US2

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: M. Hayama et al. : Art Unit:
Serial No.: To Be Assigned : Examiner:
Filed: Herewith :
For: METHOD FOR FABRICATING A :
MULTILAYER CERAMIC :
SUBSTRATE (AS AMENDED)

DIVISIONAL OF:

Applicant: M. Hayama et al. : Art Unit: 2814
Serial No.: 09/173,288 : Examiner: A. Chambliss
Filed: October 14, 1998 : Attn: Issue Branch
For: METHOD FOR FABRICATING A : Confirmation No.: 1587
MULTILAYER CERAMIC :
SUBSTRATE (AS AMENDED) :

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

S I R :

Prior to examination, please amend the above-identified application as follows:

IN THE TITLE:

Please replace the Title beginning at page 1, line 1 of the Specification:

METHOD FOR FABRICATING A MULTILAYER CERAMIC SUBSTRATE

IN THE SPECIFICATION:

Please insert the following section at page 1, line 5 of the Specification:

CROSS-RELATED APPLICATIONS

This application is a Divisional application of U.S. Patent Application Serial No. 09/173,288, filed October 14, 1998.

IN THE DRAWINGS:

Please delete sheets "5/13", "6/13", and "7/13" and replace with the figures attached hereto.

IN THE CLAIMS:

Please cancel claims 1-12.

Please replace claims 15-21 with the following amended claims:

1 15. (As Amended) The multilayer ceramic substrate of claim 13, wherein a
2 meshed pattern is provided in a part of said conductive pattern.

1 16. (As Amended) The multilayer ceramic substrate of claim 13, wherein a
2 shield pattern is provided at an outer edge of said conductive pattern.

1 17. (As Amended) The multilayer ceramic substrate of claim 13, wherein
2 said ceramic substrate is provided with a through hole filled with an
3 electroconductive substance and burned, and said via is disposed on the through
4 hole.

1 18. (As Amended) The multilayer ceramic substrate of claim 13, further
2 comprising a dielectric layer formed on a part of said ceramic substrate.

1 19. (As Amended) The multilayer ceramic substrate of claim 13, further
2 comprising an LSI chip mounted on a part of one of said first and second
3 conductive patterns with the face down and electrically connected.

1 20. (As Amended) The multilayer ceramic substrate of claim 13, further
2 comprising an LSI chip mounted on a part of one of said first and second
3 conductive patterns with the face down and electrically connected through an
4 electroconductive paste applied on the top of a fine bump provided on one of said
5 first and second conductive patterns, said fine bump formed by using a second
6 groove which is disposed on said intaglio at a place corresponding to a pad of said
7 LSI chip

1 21. (As Amended) The multilayer ceramic substrate of claim 13, further
2 comprising an LSI package mounted on a part of one of said first and second
3 conductive patterns with the face down and electrically connected through a lattice
4 of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said
5 first and second conductive patterns.

1 Please add the following new claims:

1 22. (Newly Added) The multilayer ceramic substrate of claim 14, wherein
2 a meshed pattern is provided in a part of said conductive pattern.

1 23. (Newly Added) The multilayer ceramic substrate of claim 14, wherein
2 a shield pattern is provided at an outer edge of said conductive pattern.

1 24. (Newly Added) The multilayer ceramic substrate of claim 14, wherein
2 said ceramic substrate is provided with a through hole filled with an
3 electroconductive substance and burned, and said via is disposed on the through
4 hole.

1 25. (Newly Added) The multilayer ceramic substrate of claim 14, further
2 comprising a dielectric layer formed on a part of said ceramic substrate.

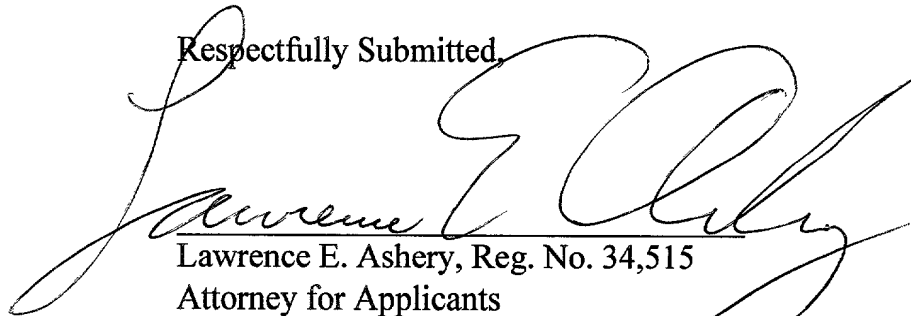
1 26. (Newly Added) The multilayer ceramic substrate of claim 14, further
2 comprising an LSI chip mounted on a part of one of said first and second
3 conductive patterns with the face down and electrically connected.

1 27. (Newly Added) The multilayer ceramic substrate of claim 14, further
2 comprising an LSI chip mounted on a part of one of said first and second
3 conductive patterns with the face down and electrically connected through an
4 electroconductive paste applied on the top of a fine bump provided on one of said

5 first and second conductive patterns, said fine bump formed by using a second
6 groove which is disposed on said intaglio at a place corresponding to a pad of said
7 LSI chip.

1 28. (Newly Added) The multilayer ceramic substrate of claim 14, further
2 comprising an LSI package mounted on a part of one of said first and second
3 conductive patterns with the face down and electrically connected through a lattice
4 of lands with a pitch of not larger than 0.8mm, said lattice provided on one of said
5 first and second conductive patterns.

Respectfully Submitted,



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Attorney for Applicants

LEA/lm

Enclosure: Version With Markings Showing Changes Made

Dated: February 12, 2002

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Commissioner for Patents, Washington, D.C. 20231.



Kathleen Libby

VERSION WITH MARKINGS TO SHOW CHANGES MADETITLE:

Specification at page 1, line 1:

~~MULTILAYER CERAMIC SUBSTRATE AND METHOD FOR~~
~~FABRICATING THE SAME~~METHOD FOR FABRICATING A MULTILAYER
CERAMIC SUBSTRATE

SPECIFICATION:

Specification at page 1, line 5:

CROSS-RELATED APPLICATIONS

This application is a Divisional application of U.S. Patent Application
Serial No. 09/173,288, filed October 14, 1998.

CLAIMS:

1 15. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or
2 claim 14], wherein a meshed pattern is provided in a part of said conductive
3 pattern.

1 16. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or
2 claim 14], wherein a shield pattern is provided at an outer edge of said conductive
3 pattern.

1 17. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or
2 claim 14], wherein said ceramic substrate is provided with a through hole filled
3 with an electroconductive substance and burned, and said via is disposed on the
4 through hole.

1 18. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or
2 claim 14], further comprising a dielectric layer formed on a part of said ceramic
3 substrate.

1 19. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or
2 claim 14], further comprising an LSI chip mounted on a part of one of said first
3 and second conductive patterns with the face down and electrically connected.

1 20. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or
2 claim 14], further comprising an LSI chip mounted on a part of one of said first
3 and second conductive patterns with the face down and electrically connected
4 through an electroconductive paste applied on the top of a fine bump provided on
5 one of said first and second conductive patterns, said fine bump formed by using a
6 second groove which is disposed on said intaglio at a place corresponding to a pad
7 of said LSI chip

1 21. (As Amended) The multilayer ceramic substrate of [either] claim 13 [or
2 claim 14], further comprising an LSI package mounted on a part of one of said first
3 and second conductive patterns with the face down and electrically connected
4 through a lattice of lands with a pitch of not larger than 0.8mm, said lattice
5 provided on one of said first and second conductive patterns.

Claims 1-12 have been cancelled.

Claims 22-28 are newly added.

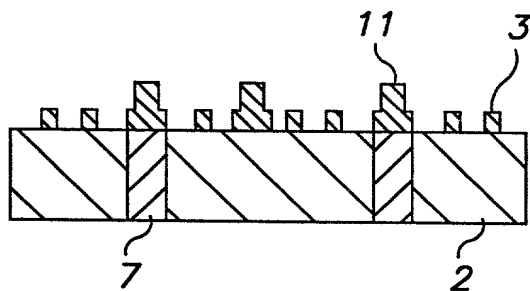


FIG. 10(a)

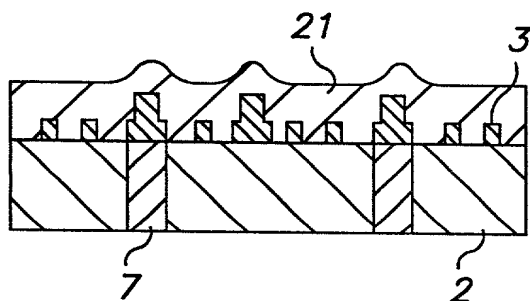


FIG. 10(b)

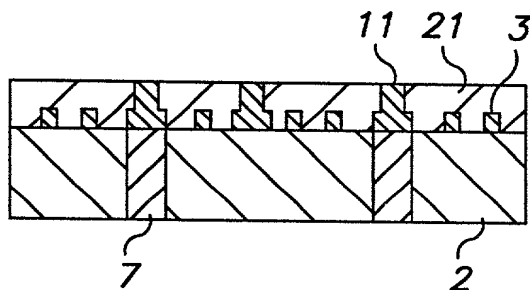


FIG. 10(c)

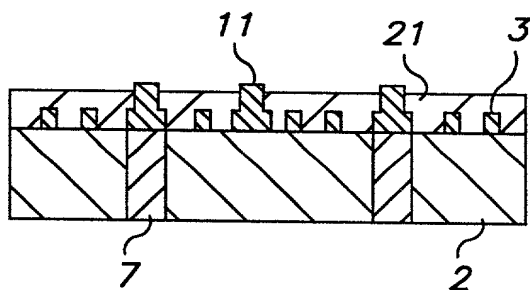


FIG. 10(d)

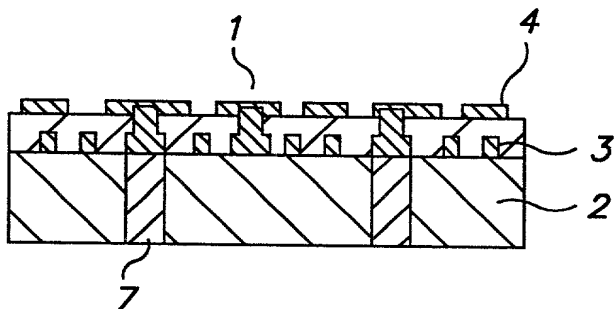


FIG. 10(e)

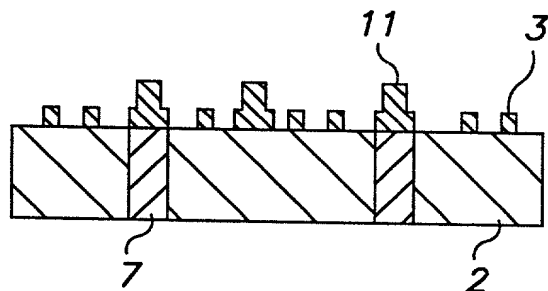


FIG. 11(a)

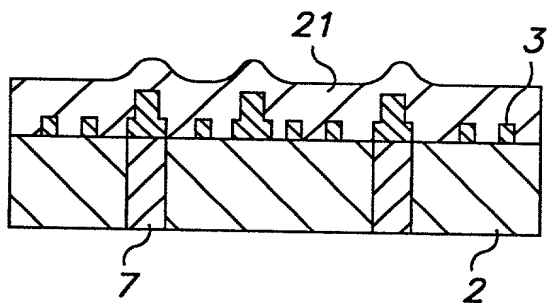


FIG. 11(b)

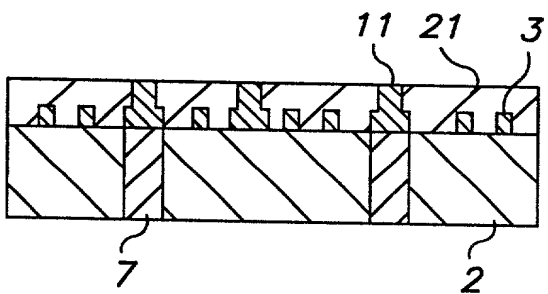


FIG. 11(c)

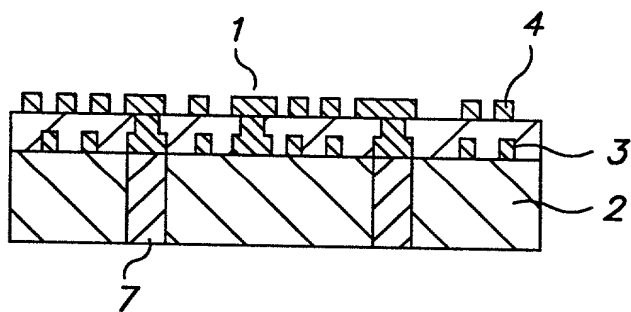


FIG. 11(d)

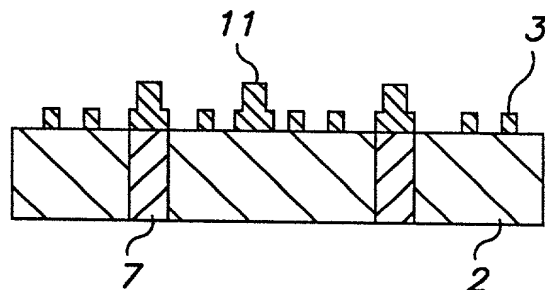


FIG. 12(a)

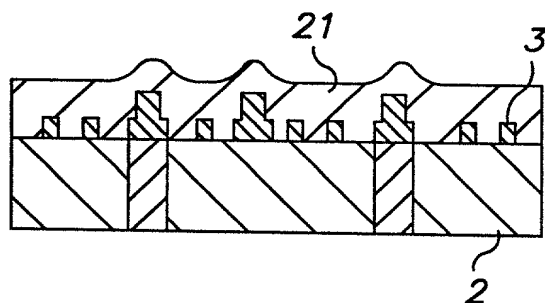


FIG. 12(b)

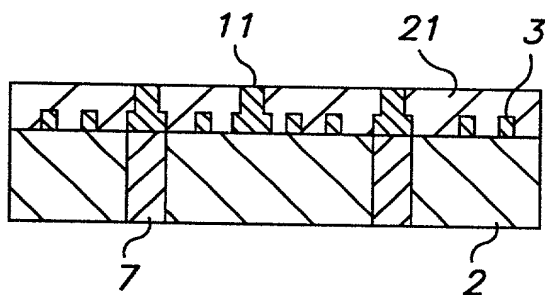


FIG. 12(c)

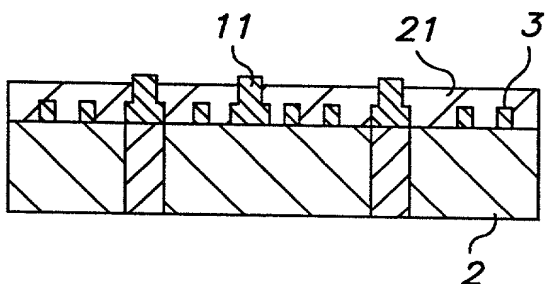


FIG. 12(d)

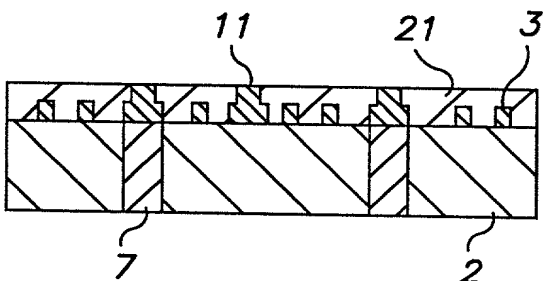


FIG. 12(e)

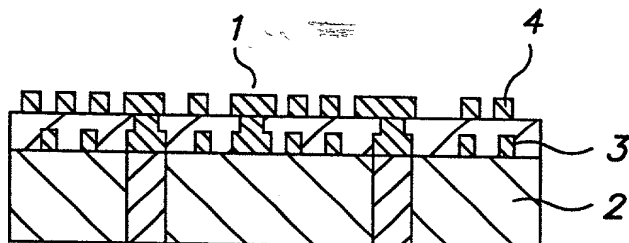


FIG. 12(f)